

In re Patent Application of:
DELLMO ET AL.
Serial No. **10/806,668**
Filed: **March 23, 2004**

REMARKS

The Examiner is thanked for the thorough examination of the present application. The Examiner is also thanked for the courtesies extended during the telephonic interview of February 1, 2010, during which the claim rejections and proposed claim amendments were discussed, and the Examiner agreed that the proposed claim amendments would define over the cited prior art. Dependent Claims 10 and 20 have been cancelled for consistency.

I. The Claimed Invention

The invention, as recited in amended independent Claim 1, for example, is directed to a cryptographic device that includes a cryptographic module and a communications module removably coupled thereto. The cryptographic module includes a first housing, a user Local Area Network (LAN) interface carried by the first housing, and a cryptographic processor carried by the first housing and coupled to the user LAN interface. The cryptographic module also includes a tamper circuit for disabling the cryptographic processor based upon tampering with the first housing. The tamper circuit includes at least one conductive trace printed on at least the inside of the first housing so that the cryptographic processor is disabled based upon a break in the at least one conductive trace. Furthermore, the communications module includes a second housing and a network wireless LAN interface carried by the second housing

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coupled to the cryptographic processor and switchable between wireless LAN modes.

Amended independent Claim 11 is directed to a similar cryptographic device, and amended independent Claims 21 and 25 are directed to related methods. Amended independent Claim 29 is directed to a related communications system. Independent Claims 11, 21, 25, and 29 have been amended similar to amended independent Claim 1.

II. The Amended Claims Are Patentable

The Examiner rejected independent Claims 1, 11, 21, 25, and 29 over Dhir et al. in view of Cheng in further view of Hamlin et al. Dhir et al. is directed to a programmable integrated circuit, namely a field programmable gate array (FPGA), that can be used to handle different wireless local area network (WLAN) communication specifications. The integrated circuit includes a transceiver coupled to programmable gates, memory coupled to the programmable gates for storing instructions for programming a first portion of the programmable gates with a selected one of a first type of a medium access layer and a second type of a medium access layer. The first type of the medium access layer is different from the second type of medium access layer, though both the first type of the medium access layer and the second type of the medium access layer are compatible with the transceiver. The memory is configured for storing instructions for programming a second

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portion of the programmable gates as a baseband controller.

(See, e.g., Col. 2, lines 14-49, of Dhir et al.).

The Examiner correctly acknowledges that Dhir et al. fails to teach a cryptographic module and a communications module that are removably coupled to one another, and a cryptographic module including a tamper circuit for disabling the cryptographic processor based upon tampering with the first housing. The Examiner then turned to Cheng for one of these critical deficiencies. Cheng is directed to an add-on card for a computer that is detachable from the computer and allows the computer to communicate with both wired and wireless networks. The add-on card includes an access control circuit, volatile and non-volatile memory, a wireless transmission module, and a network connection module. The network connection module has both an antenna for communicating with a wireless network, and a standard network cable port for connecting to a wired network. (See, e.g., paragraphs 0009-0010 of Cheng).

The Examiner still further recognized that even a selective combination of Dhir et al. and Cheng fails to disclose the cryptographic module including a tamper circuit for disabling the cryptographic processor based upon tampering with the first housing. The Examiner turned to Hamlin for this critical deficiency. Hamlin is directed to a device including encryption circuitry enabled by comparing an operating spectral signature to an initial spectral signature.

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Independent Claims 1, 11, 21, 25, and 29 have been amended to recite the tamper circuit including at least one conductive trace printed on at least the inside of the first housing so that the cryptographic processor is disabled based upon a break in the at least one conductive trace.

Applicants submit, and the Examiner agreed, that even a selective combination of the prior art fails to disclose the cryptographic module including a tamper circuit for disabling the cryptographic processor based upon tampering with the first housing, wherein the tamper circuit includes at least one conductive trace printed on at least the inside of the first housing so that the cryptographic processor is disabled based upon a break in the at least one conductive trace.

Accordingly, it is submitted that amended independent Claims 1, 11, 21, 25, and 29 are patentable over the prior art. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

III. CONCLUSION

In view of the arguments and amendments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the

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Examiner is encouraged to contact the undersigned attorney at
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Respectfully submitted,



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